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EXAMINER	
GARBOWSKI, LEIGH M	

ART UNIT	PAPER NUMBER
2825	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/071,862	HE ET AL.	
	Examiner	Art Unit	
	Leigh Marie Garbowski	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-70* is/are pending in the application.

4a) Of the above claim(s) *1-5 and 27-70* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *(04/26/2002)*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Election/Restrictions

Applicant's election with traverse of Group II claims 6-26 in the reply filed on 01/19/2005 is acknowledged. The traversal is on the ground(s) that the claim groups are misclassified and there is no serious burden on the examiner. This is not found persuasive because the claims are properly grouped and classified; each of the Groups pertains to a particularly specific area of subject matter as demonstrated in the previous office action. The inventions are subcombinations; although separate Groups recite the same preamble of routing, the features recited in each of the bodies of the Groups are distinct from each other to be separately usable as described. Examining more than one of the Groups would result in a serious burden on the examiner because of the independent and distinct concepts recited in each of the Groups. Furthermore, it is unreasonable to search for more than one invention; the claimed subject matter must be focused upon while undertaking the distinct subject matter with respect to the significant amount art in any given subclass.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 6-8, 10-11, 13-14, 16-18, 20-22, 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Pryor et al. [U.S. Patent #4,612,618]

As per claim 6, a method of routing an IC design comprising: accessing the IC design including a plurality of objects on one or more layers [column 5, lines 45-48; column 8, lines 21-24]; accessing a first level for the IC design, wherein the first level of the IC design is partitioned into a first plurality of one or more partitions, and the plurality of objects of the IC design are among the first plurality of one or more partitions [column 5, lines 49-56; column 8, lines 29-32]; and forming a second level for the IC design, including: partitioning the second level into a plurality of partitions, wherein one or more partitions of the first plurality of partitions is represented by at least two partitions of the second plurality of partitions [column 6, lines 21-29; column 8, lines 33-36]; and within each partition of the second plurality of partitions, interconnecting objects substantially independently of other partitions of the second plurality of partitions [column 6, lines 36-40; column 8, lines 36-38]. As per claim 7, wherein the routing is multithreaded at least at a first time [column 7, lines 5-8; column 8, lines 62-66]. As per claim 8, wherein the routing is single threaded at least at a first time [column 7, lines 5-8; column 8, lines 62-66]. As per claim 10, wherein every partition of the first plurality of one or more partitions has one or more objects of the plurality of objects [column 5, line 57-column 6, line 3]. As per claim 11, wherein interconnecting objects substantially independently is subject at least to boundary conditions of the second plurality of partitions [column 4, lines 8-32]. As per claim 13, wherein each partition of the first plurality of partitions is represented by at least two partitions of the second plurality of partitions [column 1, lines 60-62]. As per claim 14, wherein each of the first level, and the second level includes at least two layers [column 5, lines 38-40].

As per claim 16, a method of routing an IC design comprising: accessing the IC design including a plurality of objects on one or more layers [column 5, lines 45-48; column 8, lines 21-24]; accessing a first level for the IC design, wherein the first level of the IC design is partitioned into a first plurality of one or more partitions, and the plurality of objects of the IC design are among the first plurality of one or more partitions [column 5, lines 49-56; column 8, lines 29-32]; and forming a second level for the IC design, including: partitioning the second level into a plurality of partitions, wherein one or more partitions of the first plurality of partitions is represented by at least two partitions of the

second plurality of partitions [column 6, lines 21-29; column 8, lines 33-36]; allotting the second plurality of partitions among a plurality of areas, such that each area of the plurality of areas includes one or more partitions of the second plurality of partitions [column 4, line 34; column 6, lines 21-29; column 8, lines 33-36]; and within each area of the plurality of areas, interconnecting objects substantially independently of other areas of the plurality of areas [column 6, lines 36-40; column 8, lines 36-38]. As per claim 17, wherein the routing is multithreaded at least at a first time [column 7, lines 5-8; column 8, lines 62-66]. As per claim 18, wherein the routing is single threaded at least at a first time [column 7, lines 5-8; column 8, lines 62-66]. As per claim 20, wherein every partition of the first plurality of one or more partitions has one or more objects of the plurality of objects [column 5, line 57-column 6, line 3]. As per claim 21, wherein interconnecting objects substantially independently is subject at least to boundary conditions of the second plurality of partitions [column 4, lines 8-32]. As per claim 22, wherein interconnecting objects substantially independently is subject at least to boundary conditions of the plurality of areas [column 4, lines 8-32]. As per claim 25, wherein each of the first level, and the second level includes at least two layers [column 5, lines 38-40].

Claims 6-11, 13-14, 16-22, 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Ting [U.S. Patent #5,640,327].

As per claim 6, a method of routing an IC design comprising: accessing the IC design including a plurality of objects on one or more layers [column 4, lines 26-28]; accessing a first level for the IC design, wherein the first level of the IC design is partitioned into a first plurality of one or more partitions, and the plurality of objects of the IC design are among the first plurality of one or more partitions [column 1, lines 59-61; column 4, lines 35-46]; and forming a second level for the IC design, including: partitioning the second level into a plurality of partitions, wherein one or more partitions of the first plurality of partitions is represented by at least two partitions of the second plurality of partitions [column 1, lines 61-63; column 4, lines 35-46]; and within each partition of the second plurality of partitions, interconnecting objects substantially independently of other partitions of the second plurality of partitions [column 2, lines 8-

10; column 4, lines 46-49]. As per claim 7, wherein the routing is multithreaded at least at a first time [column 3, lines 14-15]. As per claim 8, wherein the routing is single threaded at least at a first time [figure 2]. As per claim 9, wherein one or more partitions of the first plurality of one or more partitions has no objects of the plurality of objects [column 1, line 66-column 2, line 1]. As per claim 10, wherein every partition of the first plurality of one or more partitions has one or more objects of the plurality of objects [column 1, lines 60-61]. As per claim 11, wherein interconnecting objects substantially independently is subject at least to boundary conditions of the second plurality of partitions [column 4, lines 12-14; 26-32]. As per claim 13, wherein each partition of the first plurality of partitions is represented by at least two partitions of the second plurality of partitions [column 3, lines 55-58]. As per claim 14, wherein each of the first level, and the second level includes at least two layers [column 9, lines 55-57].

As per claim 16, a method of routing an IC design comprising: accessing the IC design including a plurality of objects on one or more layers [column 4, lines 26-28]; accessing a first level for the IC design, wherein the first level of the IC design is partitioned into a first plurality of one or more partitions, and the plurality of objects of the IC design are among the first plurality of one or more partitions [column 1, lines 59-61; column 4, lines 35-46]; and forming a second level for the IC design, including: partitioning the second level into a plurality of partitions, wherein one or more partitions of the first plurality of partitions is represented by at least two partitions of the second plurality of partitions [column 1, lines 61-63; column 4, lines 35-46]; allotting the second plurality of partitions among a plurality of areas, such that each area of the plurality of areas includes one or more partitions of the second plurality of partitions [column 1, lines 64-65; column 4, lines 37-46; column 5, lines 47-50]; and within each area of the plurality of areas, interconnecting objects substantially independently of other areas of the plurality of areas [column 2, lines 8-10; column 4, lines 46-49]. As per claim 17, wherein the routing is multithreaded at least at a first time [column 3, lines 14-15]. As per claim 18, wherein the routing is single threaded at least at a first time [figure 2]. As per claim 19, wherein one or more partitions of the first plurality of one or more partitions has no objects of the plurality of objects [column 1, line 66-column 2, line 1].

As per claim 20, wherein every partition of the first plurality of one or more partitions has one or more objects of the plurality of objects [column 1, lines 60-61]. As per claim 21, wherein interconnecting objects substantially independently is subject at least to boundary conditions of the second plurality of partitions [column 4, lines 12-14; 26-32]. As per claim 22, wherein interconnecting objects substantially independently is subject at least to boundary conditions of the plurality of areas [column 4, lines 12-14; 26-32]. As per claim 25, wherein each of the first level, and the second level includes at least two layers [column 9, lines 55-57].

Claims 6-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Pavisic et al. [U.S. Patent #6,269,469 B1].

As per claim 6, a method of routing an IC design comprising: accessing the IC design including a plurality of objects on one or more layers [column 6, lines 32-35]; accessing a first level for the IC design, wherein the first level of the IC design is partitioned into a first plurality of one or more partitions, and the plurality of objects of the IC design are among the first plurality of one or more partitions [column 2, lines 46-63; column 6, lines 40-48]; and forming a second level for the IC design, including: partitioning the second level into a plurality of partitions, wherein one or more partitions of the first plurality of partitions is represented by at least two partitions of the second plurality of partitions [column 2, lines 46-63; column 6, lines 40-48]; and within each partition of the second plurality of partitions, interconnecting objects substantially independently of other partitions of the second plurality of partitions [column 3, lines 19-22; column 6, lines 49-65]. As per claim 7, wherein the routing is multithreaded at least at a first time [column 19, lines 35-67]. As per claim 8, wherein the routing is single threaded at least at a first time [column 19, lines 35-67; column 22, lines 53-54]. As per claim 9, wherein one or more partitions of the first plurality of one or more partitions has no objects of the plurality of objects [column 2, lines 46-63]. As per claim 10, wherein every partition of the first plurality of one or more partitions has one or more objects of the plurality of objects [column 2, lines 46-63]. As per claim 11, wherein interconnecting objects substantially independently is subject at least to boundary conditions of the second plurality of partitions [column 8, lines 22-27; column 18, line 65-column 19, line

34]. As per claim 12, wherein interconnecting objects substantially independently is subject at least to a first partition of the second plurality of partitions locking at least a net shared by at least the first partition and a second partition of the second plurality of partitions to prevent a change of the net by the second partition of the second plurality of partitions [column 35, line 50-column 36, line 57]. As per claim 13, wherein each partition of the first plurality of partitions is represented by at least two partitions of the second plurality of partitions [column 2, lines 46-63]. As per claim 14, wherein each of the first level, and the second level includes at least two layers [column 1, lines 35-42; column 2, lines 7-11; 36-40]. As per claim 15, wherein each of the first level, and the second level includes one layer [column 2, lines 7-11; 36-40].

As per claim 16, a method of routing an IC design comprising: accessing the IC design including a plurality of objects on one or more layers [column 6, lines 32-35]; accessing a first level for the IC design, wherein the first level of the IC design is partitioned into a first plurality of one or more partitions, and the plurality of objects of the IC design are among the first plurality of one or more partitions [column 2, lines 46-63; column 6, lines 40-48]; and forming a second level for the IC design, including: partitioning the second level into a plurality of partitions, wherein one or more partitions of the first plurality of partitions is represented by at least two partitions of the second plurality of partitions [column 2, lines 46-63; column 6, lines 40-48]; allotting the second plurality of partitions among a plurality of areas, such that each area of the plurality of areas includes one or more partitions of the second plurality of partitions [column 2, line 64-column 3, lines 18; column 6, lines 40-48]; and within each area of the plurality of areas, interconnecting objects substantially independently of other areas of the plurality of areas [column 3, lines 19-22; column 6, lines 49-65]. As per claim 17, wherein the routing is multithreaded at least at a first time [column 19, lines 35-67]. As per claim 18, wherein the routing is single threaded at least at a first time [column 19, lines 35-67; column 22, lines 53-54]. As per claim 19, wherein one or more partitions of the first plurality of one or more partitions has no objects of the plurality of objects [column 2, lines 46-63]. As per claim 20, wherein every partition of the first plurality of one or more partitions has one or more objects of the plurality of objects [column 2, lines 46-63]. As

per claim 21, wherein interconnecting objects substantially independently is subject at least to boundary conditions of the second plurality of partitions [column 8, lines 22-27; column 18, line 65-column 19, line 34]. As per claim 22, wherein interconnecting objects substantially independently is subject at least to boundary conditions of the plurality of areas [column 8, lines 22-27; column 18, line 65-column 19, line 34]. As per claim 23, wherein interconnecting objects substantially independently is subject at least to a first partition of the second plurality of partitions locking at least a net shared by at least the first partition and a second partition of the second plurality of partitions to prevent a change of the net by the second partition of the second plurality of partitions [column 35, line 50-column 36, line 57]. As per claim 24, wherein interconnecting objects substantially independently is subject at least to a first area of the plurality of areas locking at least a net shared by at least the first area and a second area of the plurality of areas to prevent a change of the net by the second area of the plurality of areas [column 35, line 50-column 36, line 57]. As per claim 25, wherein each of the first level, and the second level includes at least two layers [column 1, lines 35-42; column 2, lines 7-11; 36-40]. As per claim 26, wherein each of the first level, and the second level includes one layer [column 2, lines 7-11; 36-40].

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Igusa et al. [U.S. Patent #6,249,902 B1] disclose multiple levels of partitioning [see figures 3A-F] including placement routability limitations. Pileggi et al. [U.S. Patent #6,651,232 B1] disclose DME for balanced routing including partitioning [see figure 2]. Heath et al. [U.S. Patent #4,688,072] disclose levels of clusters and interconnects between [column 3, lines 20-22; column 4, lines 40-54; column 5, lines 6-11, 20-31; column 7, lines 4-7].Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leigh Marie Garbowski whose telephone number is 571-272-1893 and e-mail is Leigh.Garbowski@uspto.gov. The examiner can normally be reached on days.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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PRIMARY EXAMINER